

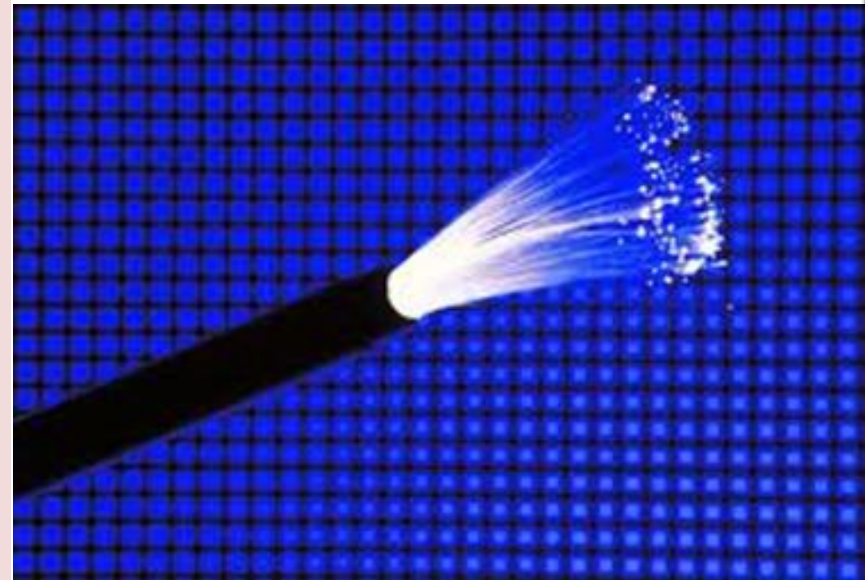
High end routing platform using optical interconnects

Kobi Hasharoni

July 2013

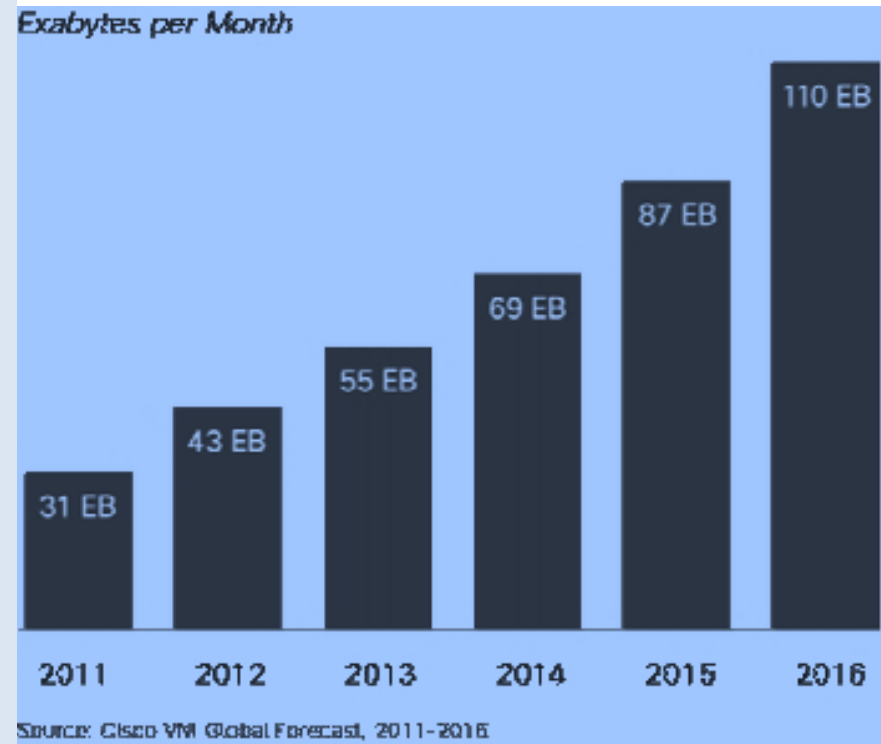
Outline

- Introduction
- The router bottleneck problem
- The solution - photonics
- The compass solution using optical interconnects



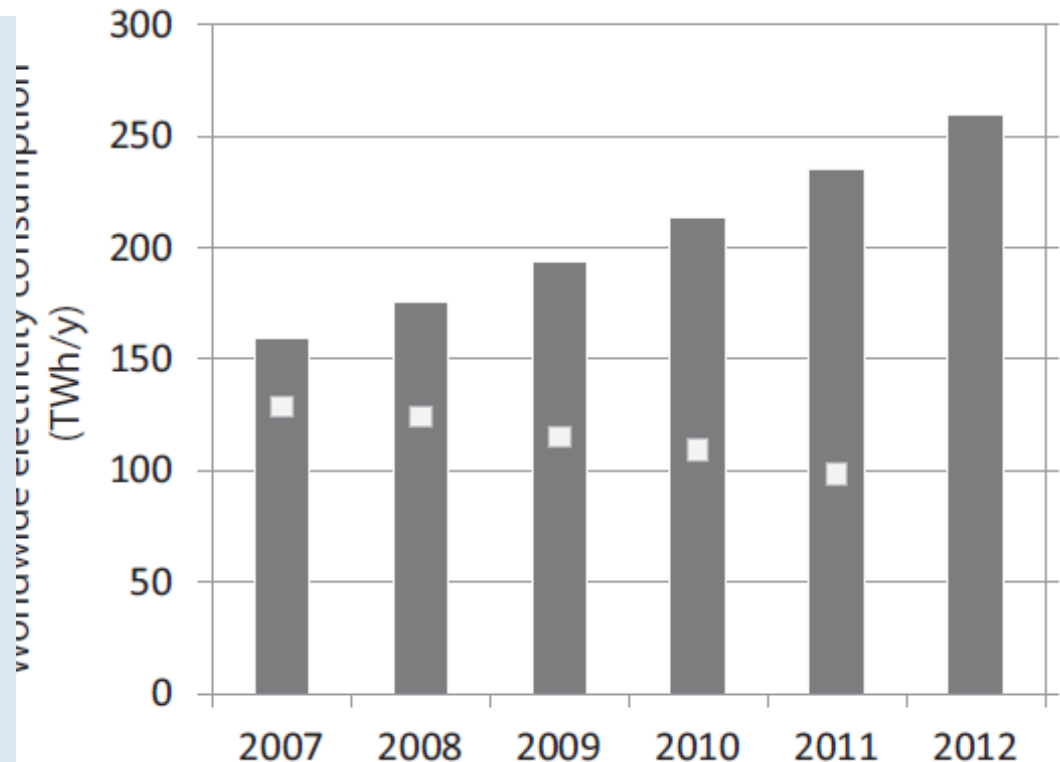
The exploding demand for BW

- With the penetration of FTTx, Mobility and Video, the **demand** for BW continues to **accelerate**.
- Yet today's network infrastructure has already **maxed out** in terms of **size, BW, power, high cost and weight**.
- Current vendors offer no solution that will allow to scale forward.
- An order of magnitude improvement is required



The price to pay 1: Power

- ❑ The total electricity consumption of routers will exceed 350TW/h/y in 2013
- ❑ This amounts to about 2% of the total electrical power in the world!
- ❑ However, the growth rate of ICT is ~40% annually!
- ❑ Core routers are responsible for most of the power consumption in ICT



Worldwide electricity consumption in telecom operator networks (S. Lambert et. al., Optic Express Vol. 20 2012)

The price to pay 2: Size & Weight

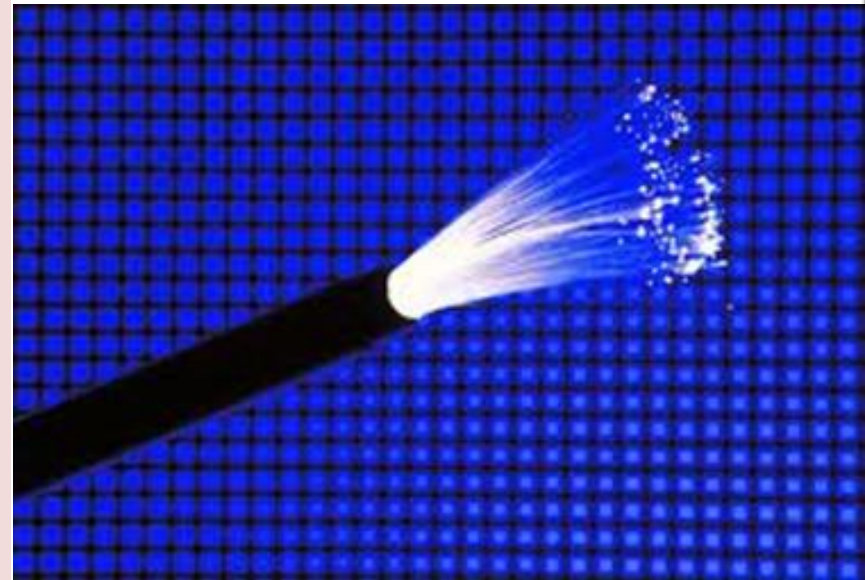


- Weight: 740 kg
- H×W×D: 2.1×0.6×1 m

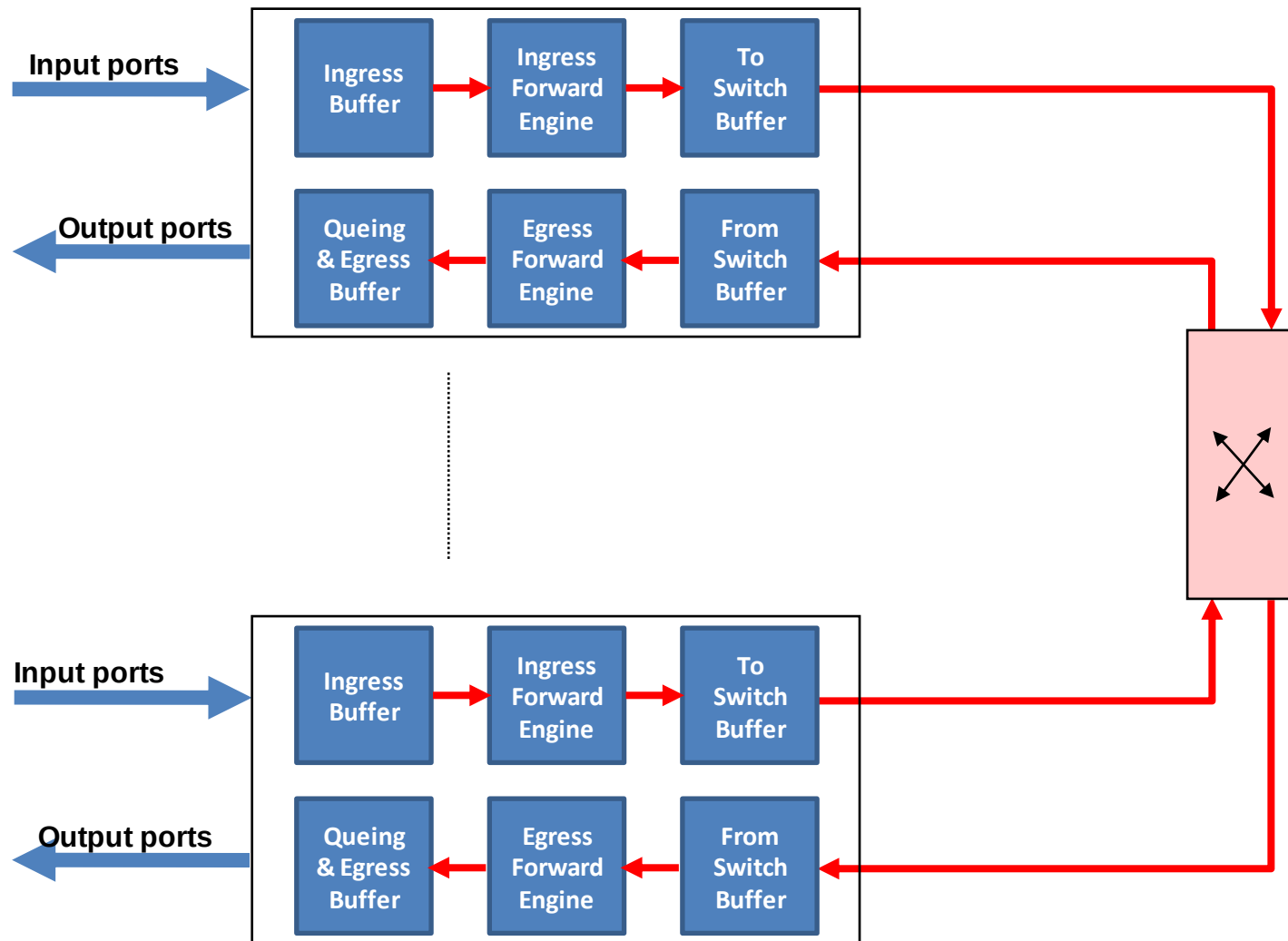
- 275 kg
- 0.44×0.95×0.78 m

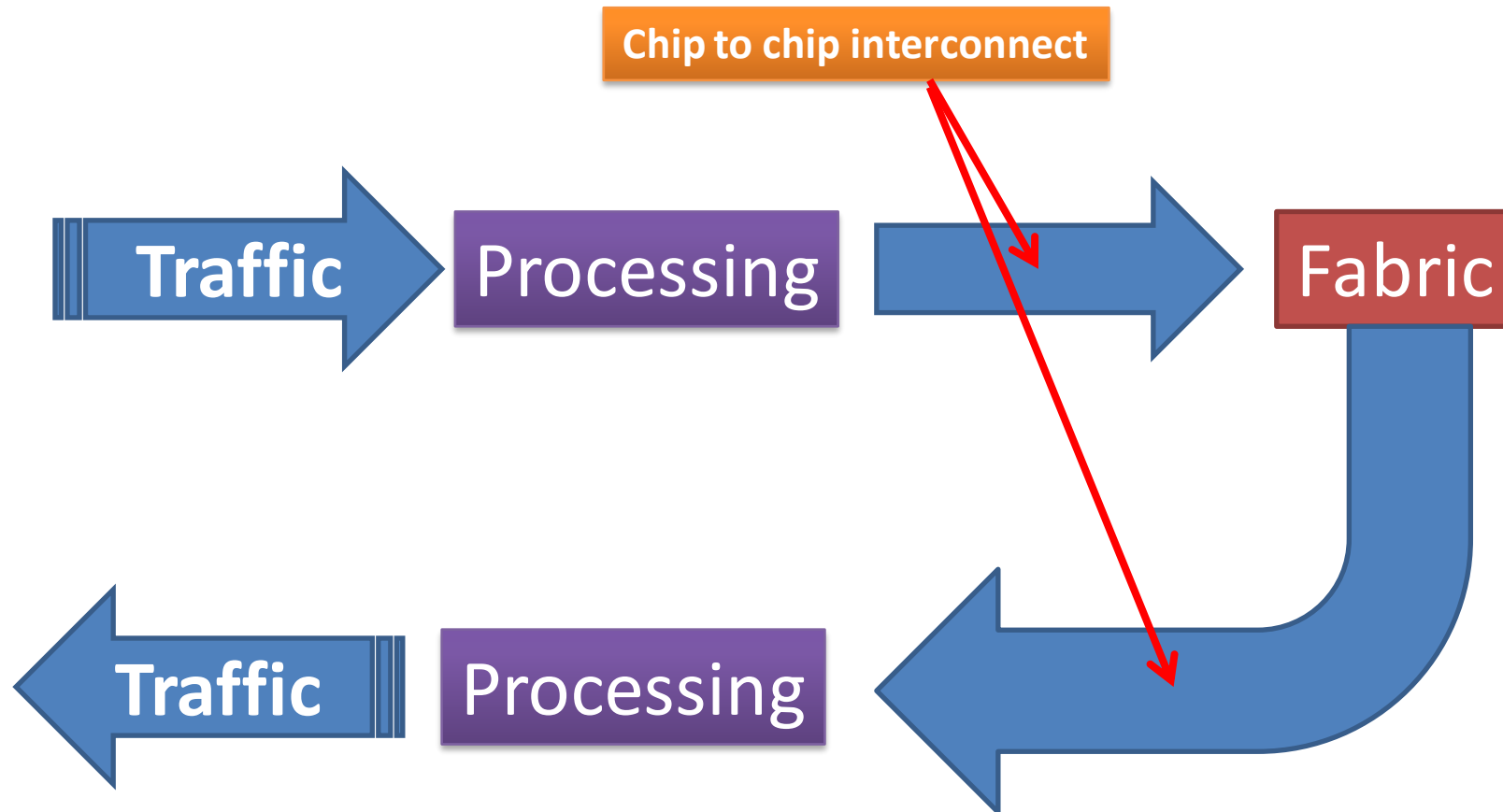
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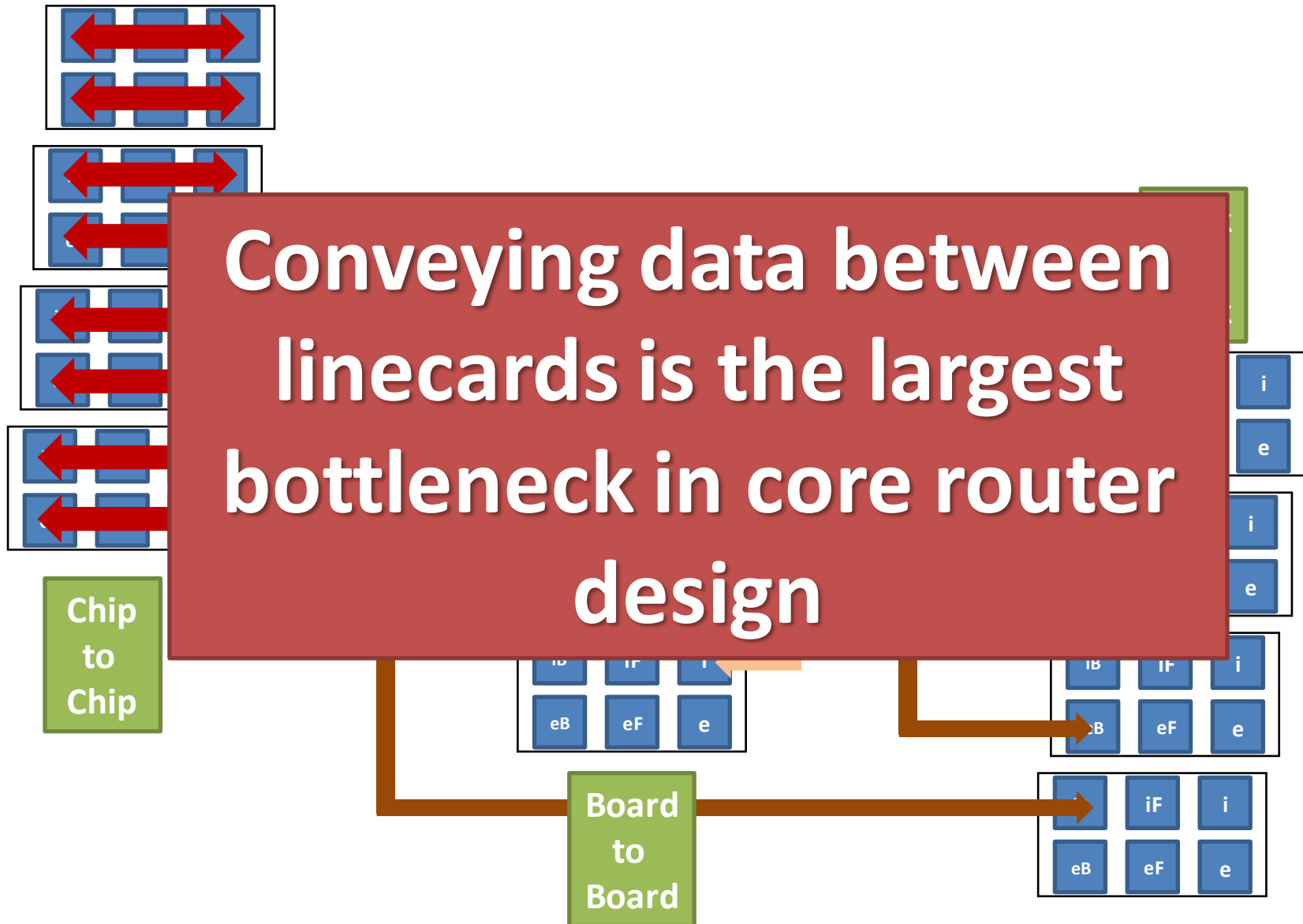


Router Architecture (1)

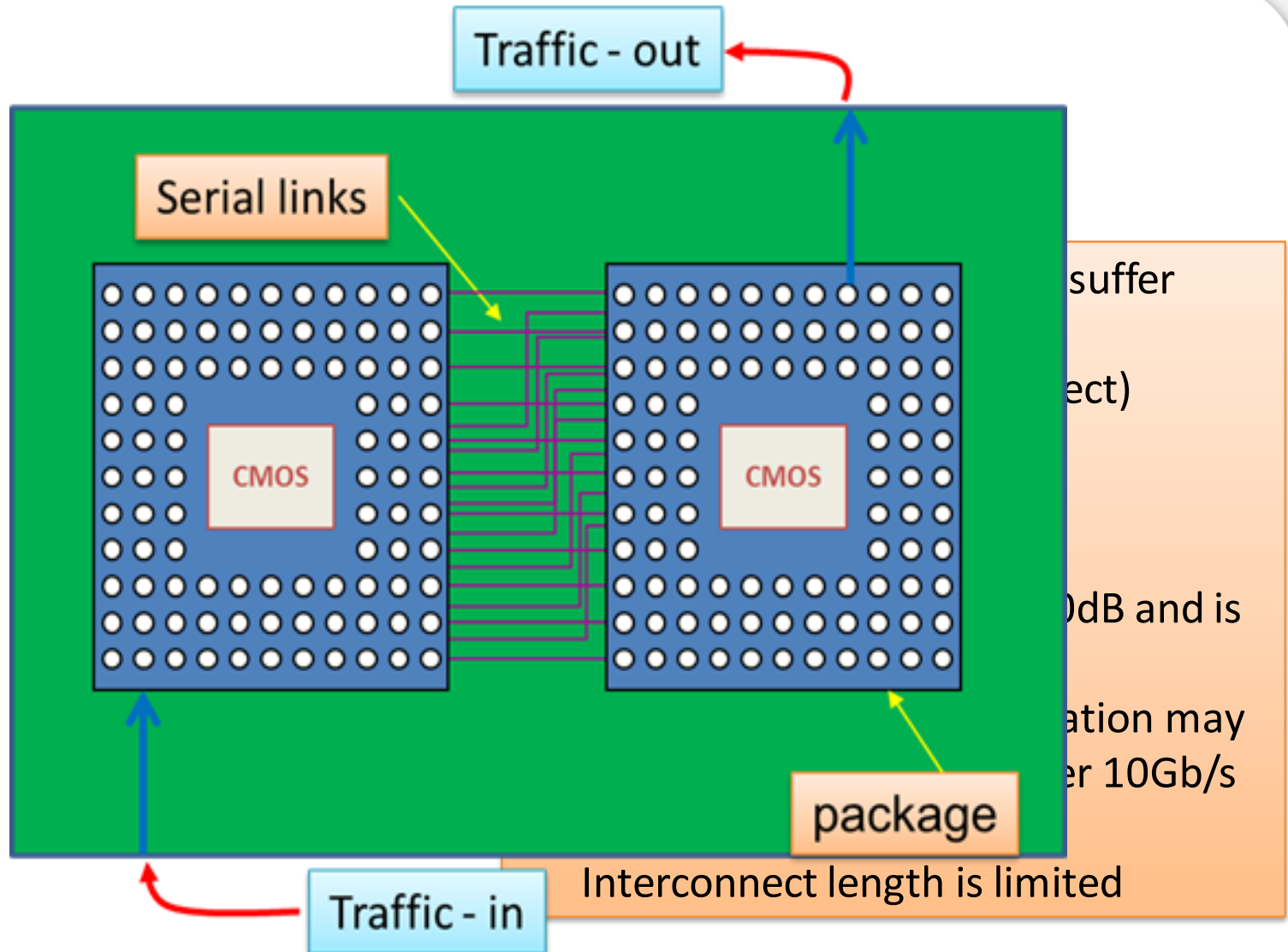




Router Architecture (2)

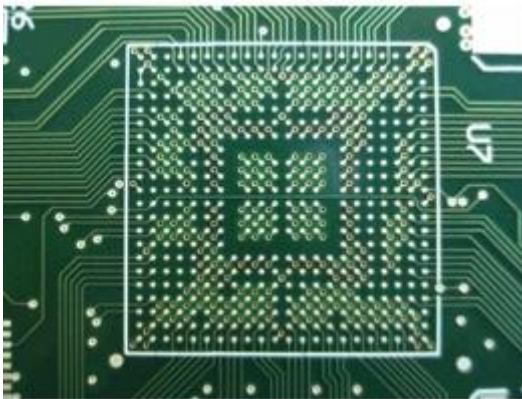


Problem #1: connectivity



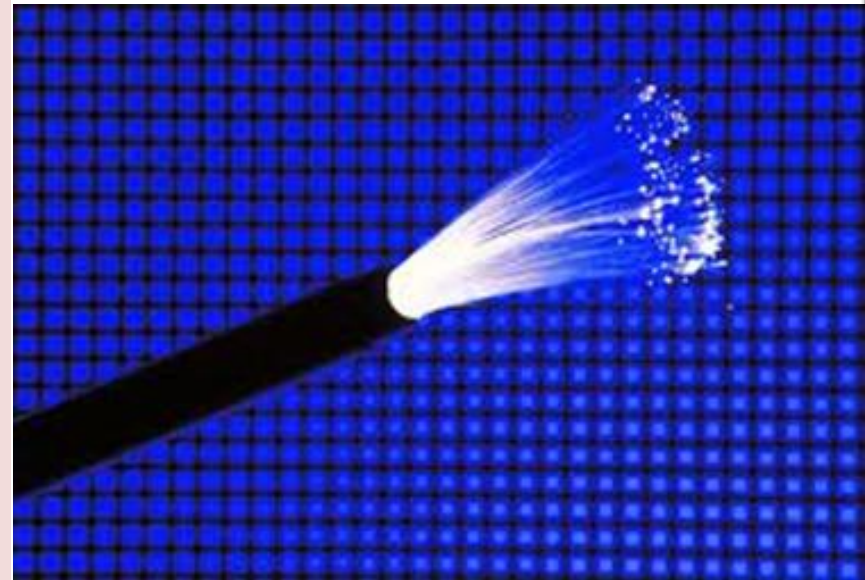
Problem #2: density

- **Q:** How do you get all of the needed BW into a single CMOS chip?
- **A:** Not with BGA technology, its limited in scale and has run out of capacity.
 - Option 1: split the data into several CMOS chips
 - Option 2: push the limit of electrical SerDes to very high data rates using 20nm CMOS or lower (?)
 - **Even if you push the limit, you cannot drive high frequency signals efficiently on the PCB!**



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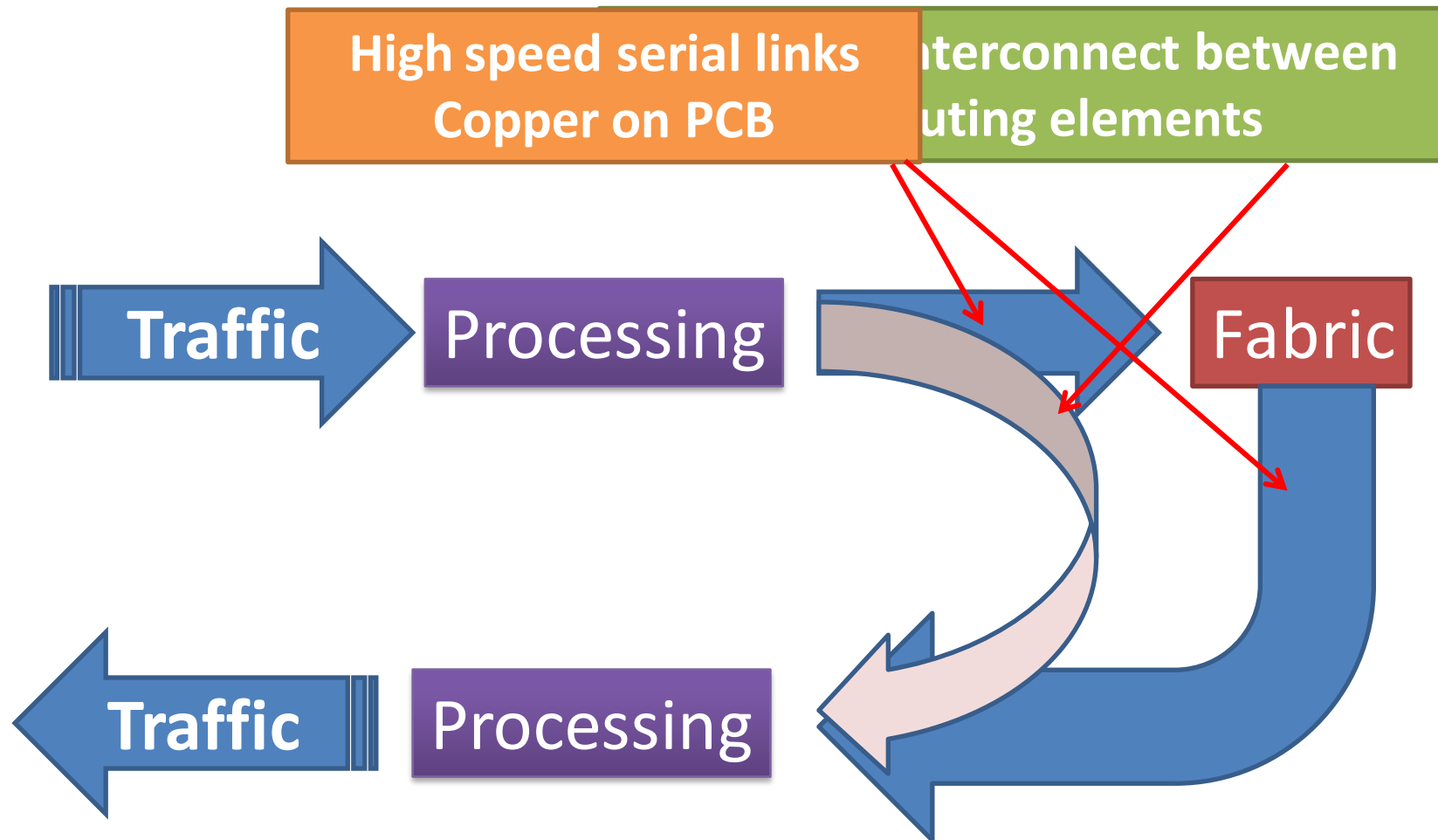


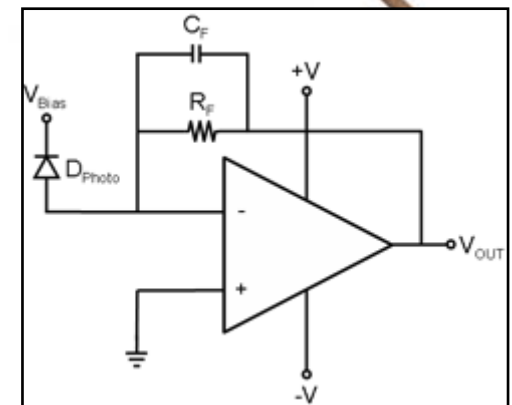
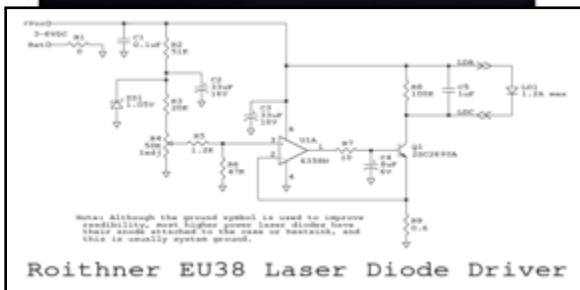
Photonics Advantages

- Insensitive to data rate
- Small power consumption
- Negligible crosstalk
- 300m serial link, $<1\text{dB/km}$ loss (multimode optics)
- Efficiency is high if using parallel links
- Minimal footprint on the CMOS chip

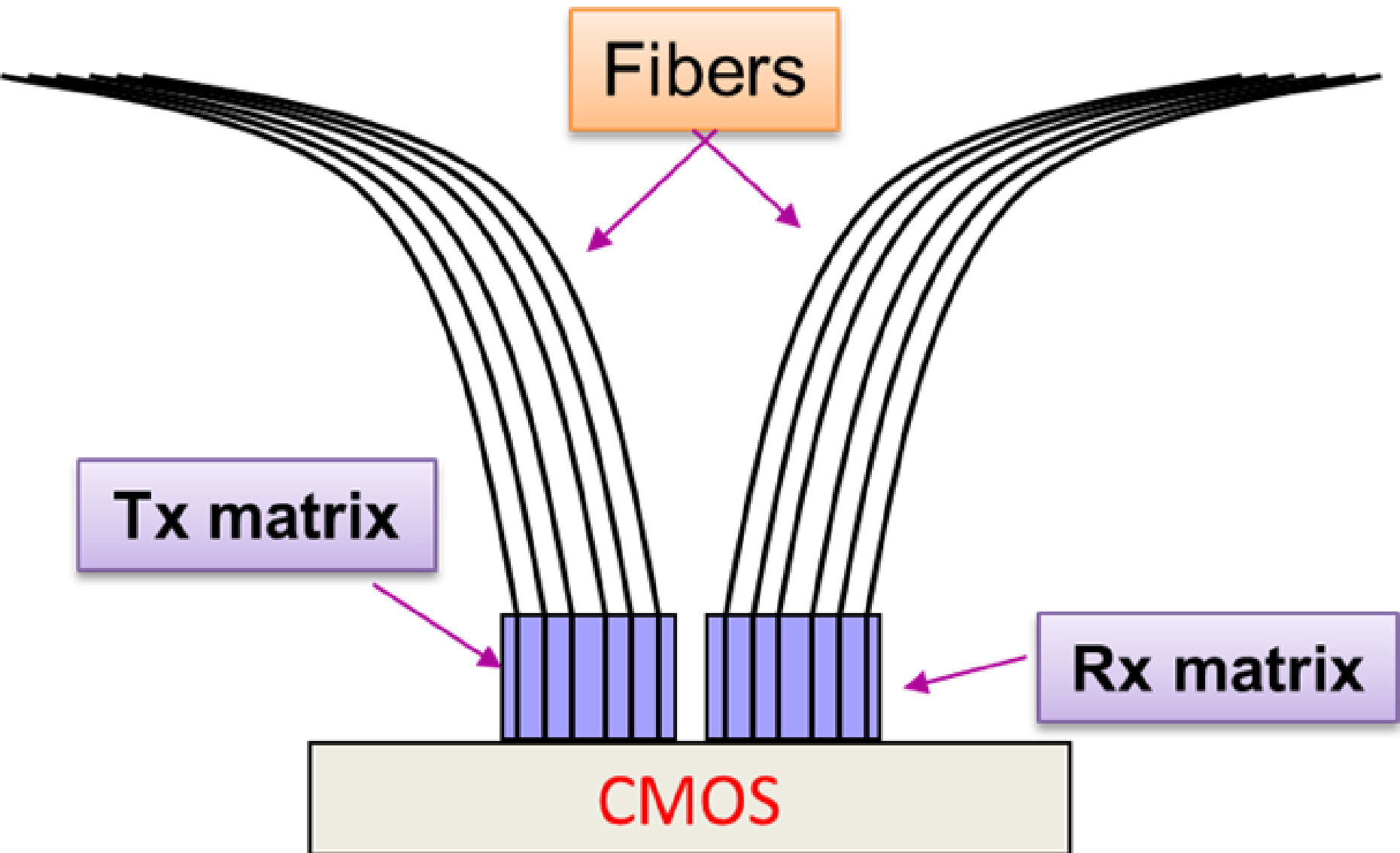


From Copper to Photons



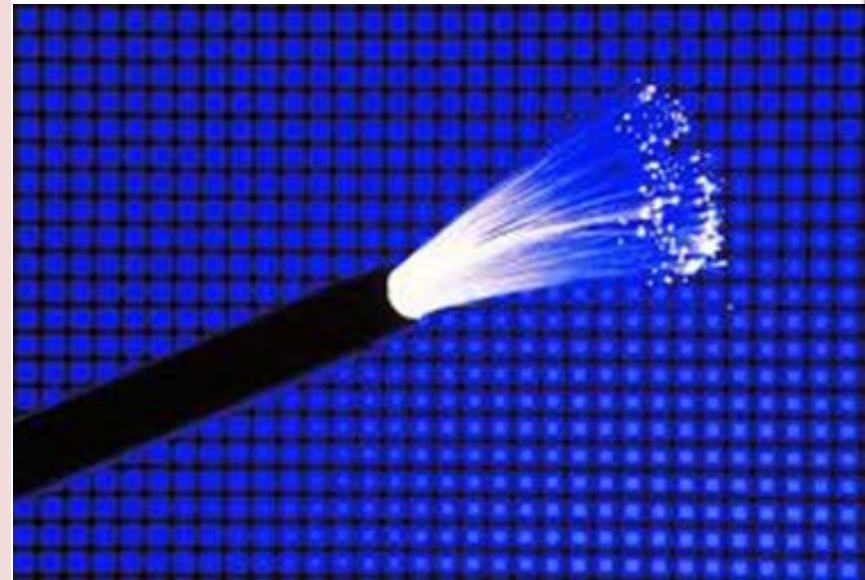


An optical interconnect-based router

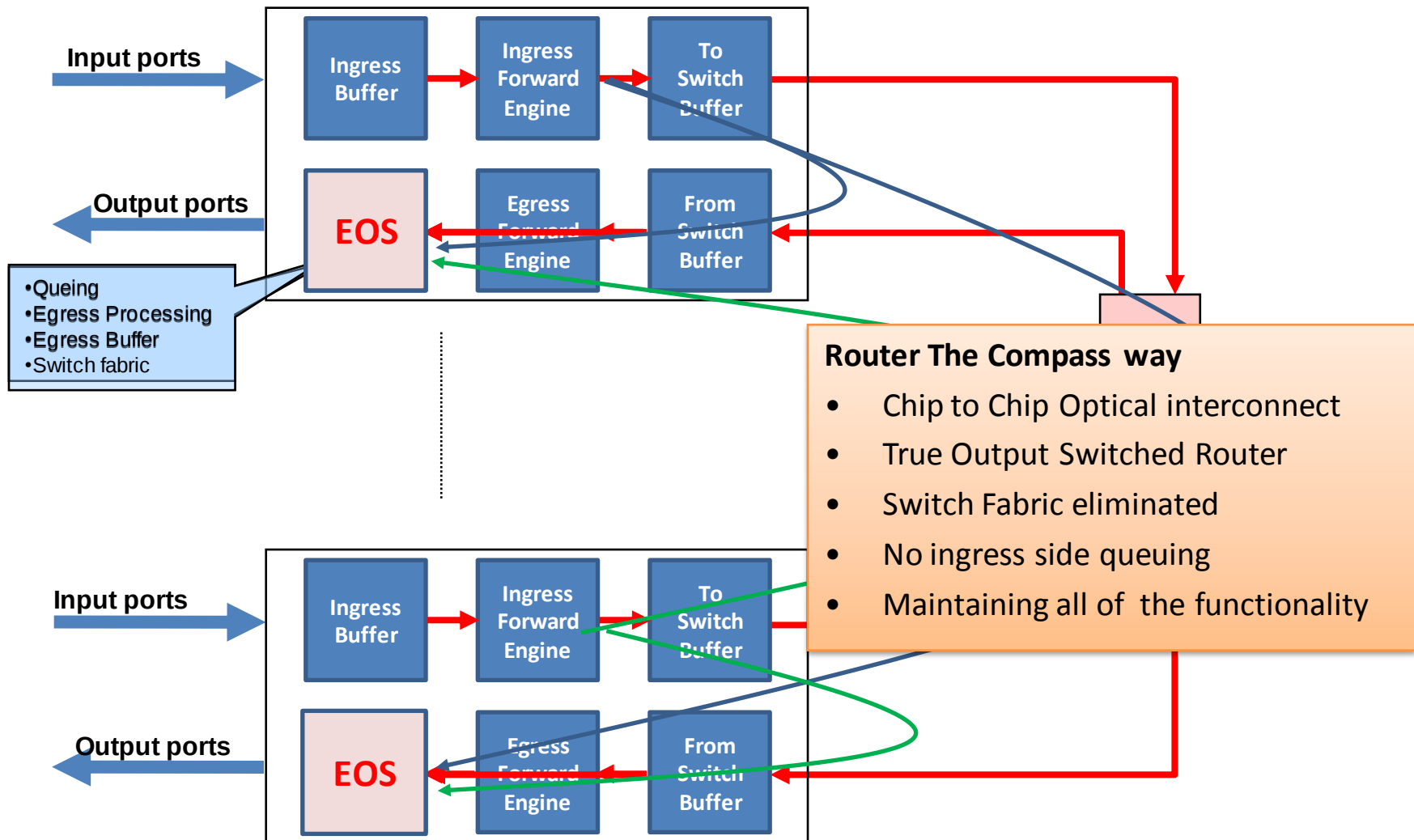


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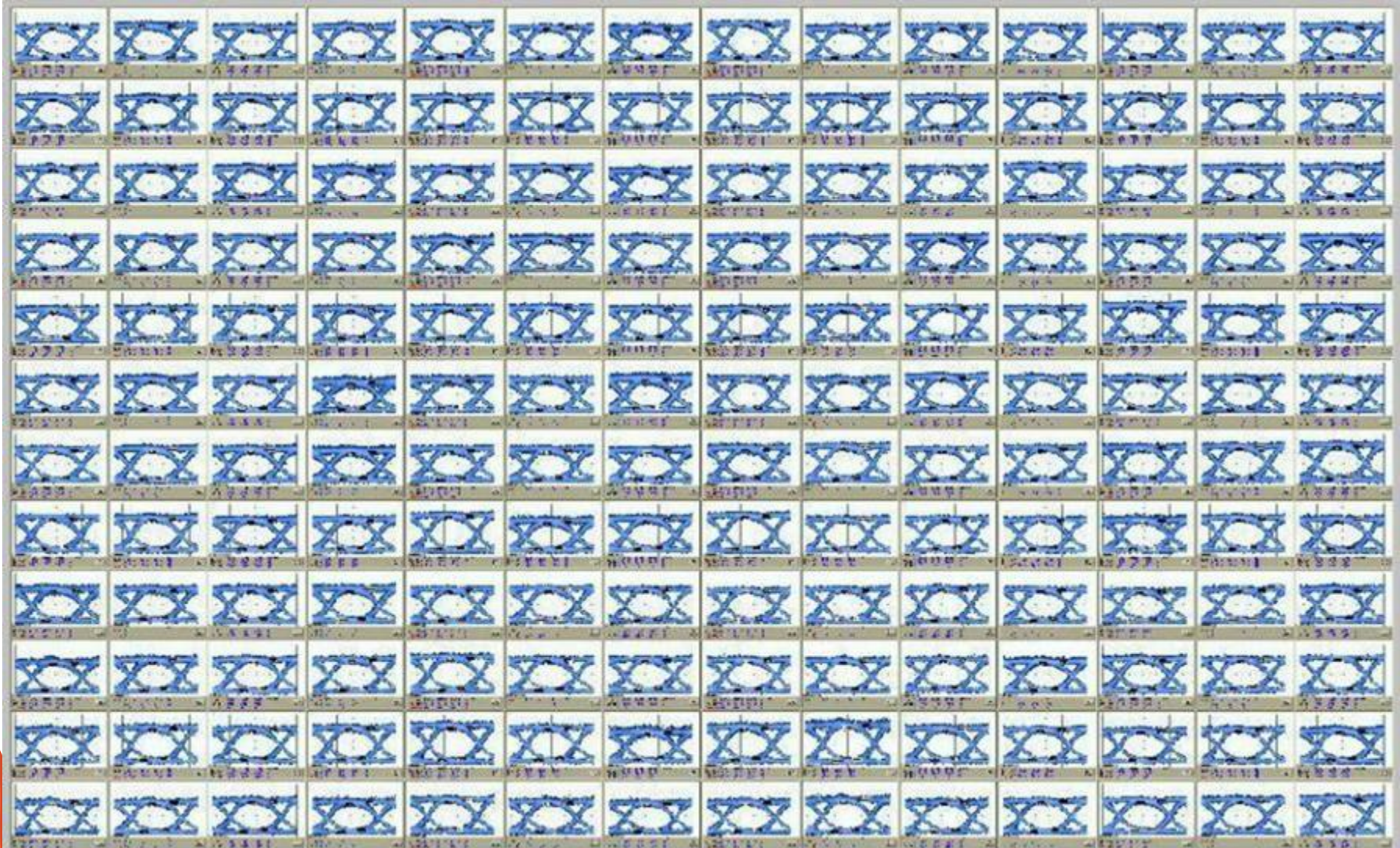


A New Router Architecture



Building an optical interconnect

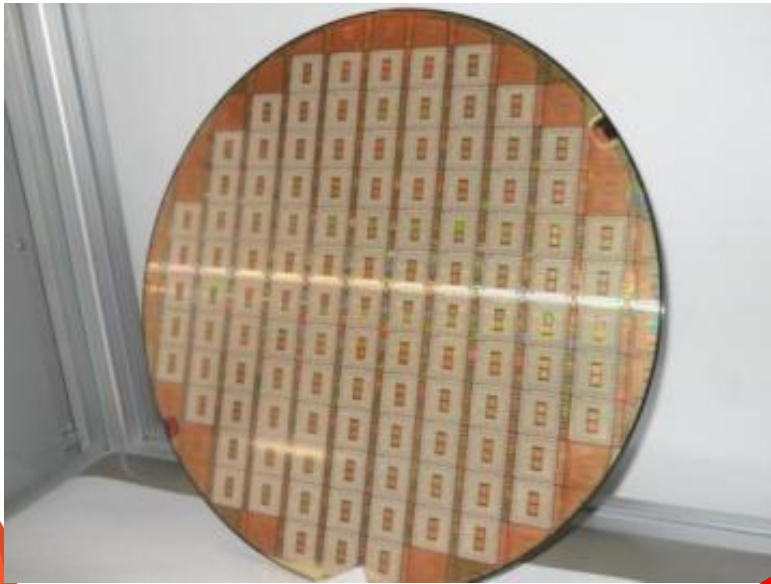
Step 1: optoelectronic chips



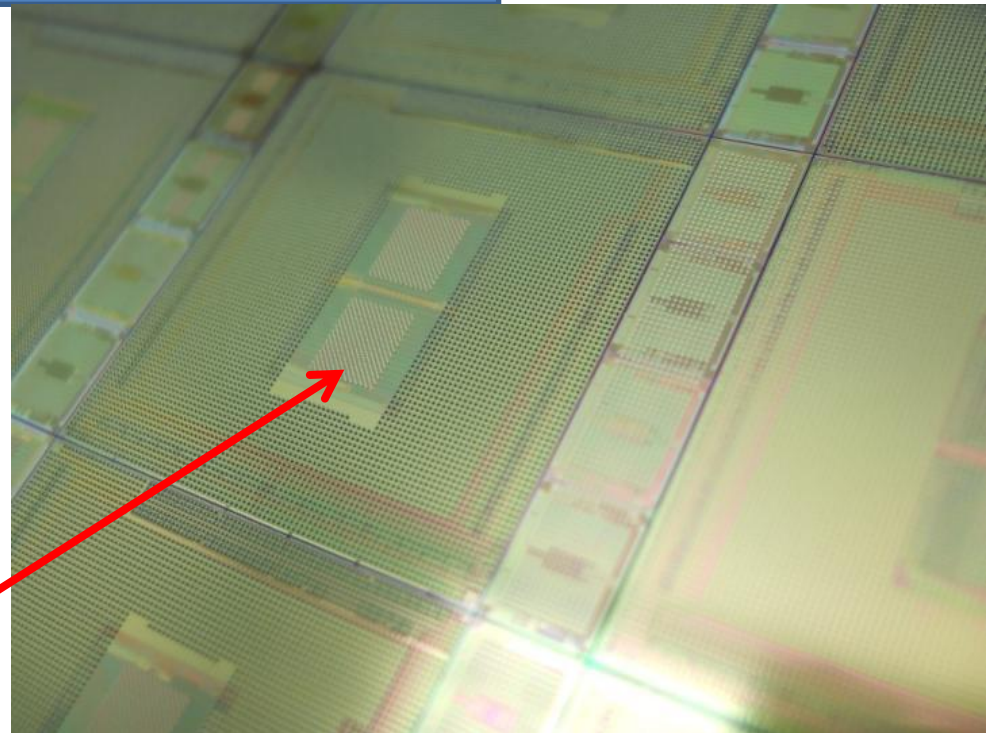
Building an optical interconnect

Step 2: Design a new CMOS

- Queing
- Egress processing
- Egress buffer
- Switch fabric
- Optical transceiver

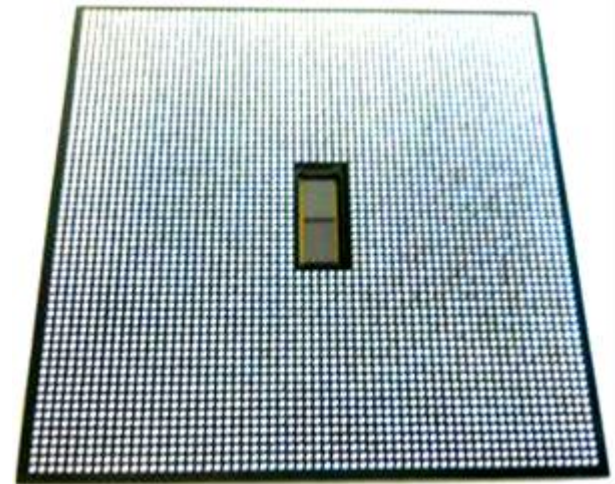
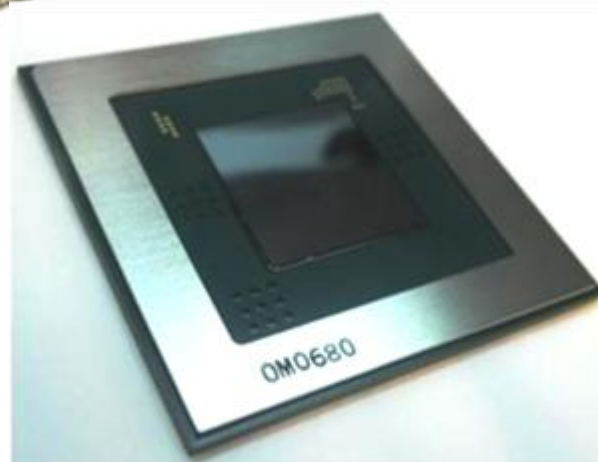
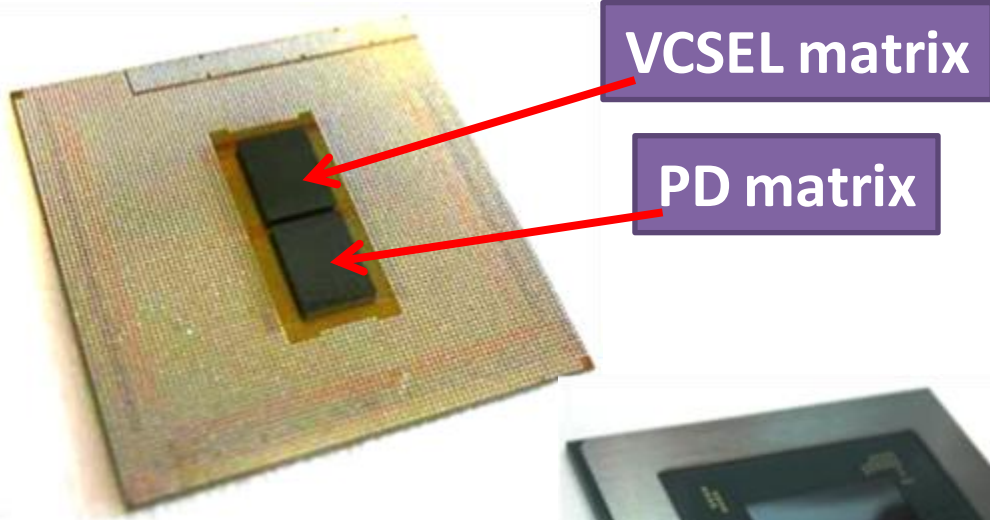


Analog circuits



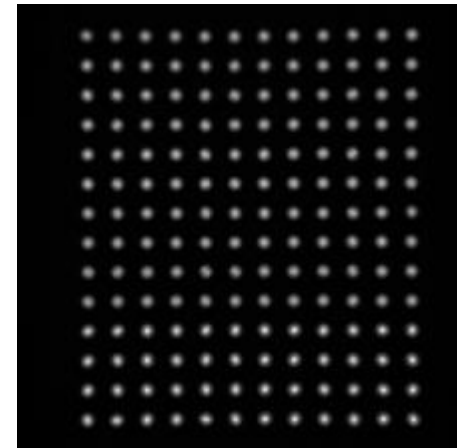
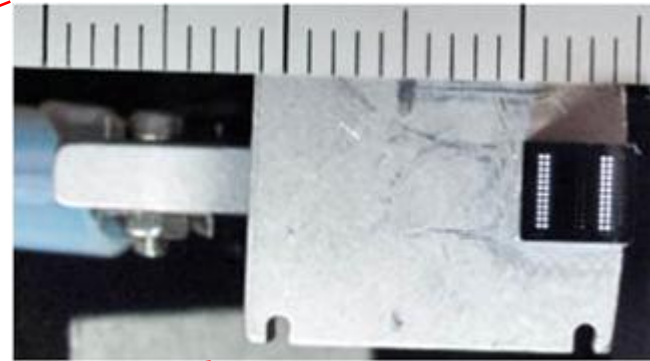
Building an optical interconnect

Step 3: assemble optics on chip



Building an optical interconnect

Step 4: build a 12×14 fiber matrix



Building an optical interconnect

Step 5: assemble optics on PCB



Building an optical interconnect

Step 6: Integrate with linecard and build a high end core router



Building an optical interconnect

- The optical interconnect enables a new class of core and edge routers:
 - Lower power consumption
 - Smaller size
 - Lower weight
 - High BW utilization
 - **Lower cost**
- Highest aggregate bandwidth reported for an optical interconnect: 1.34Tb/s full duplex
- Data density: 64Gb/s/mm²
- 168 bi-directional 8Gb/s data links
- Power efficiency: 10.2 pJ/bit (including SERDES)

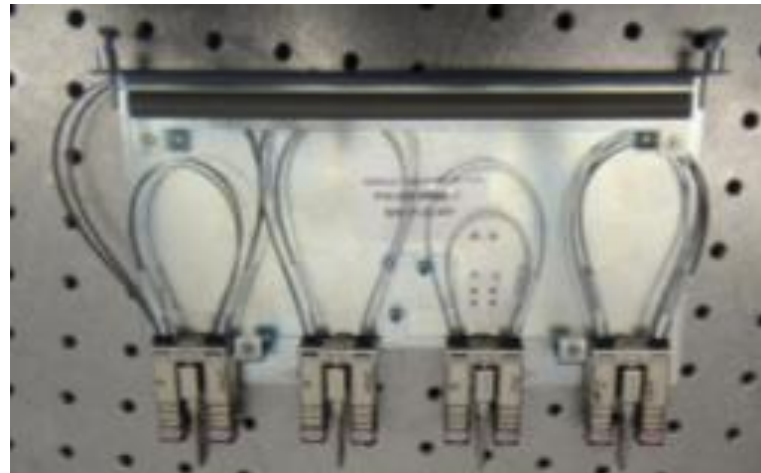
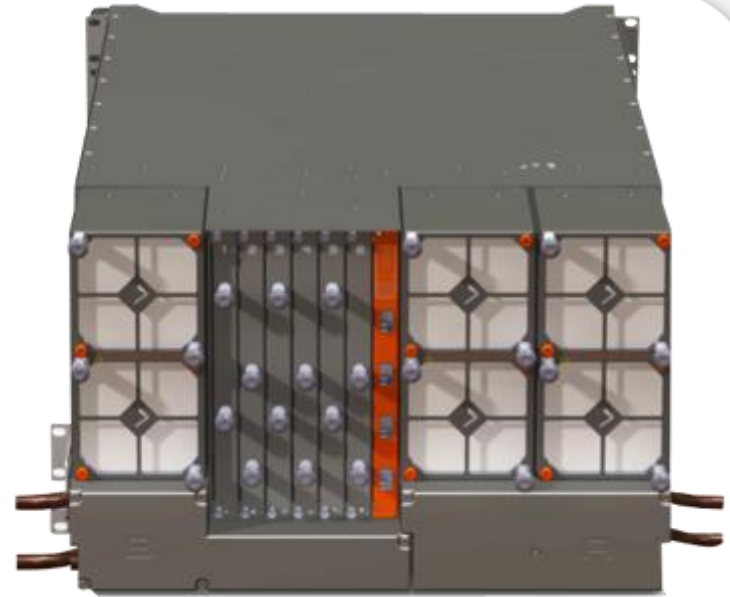
The Compass EOS core router

- 800 Gbps system
- 6 RU , 19" shelf
- 4 x Line Cards
- 3 kW
- Optical BP
- Front to Back air flow
- Distributed DC Power Supply
- Carrier Grade
- Full L3 functionality
- Multi-chassis support
- 80x10GE, 8x100GE
- Configurable 10GE/OC192/OTN



The Compass EOS core router

- Redundant power feeds
- Redundant cooling system
- Multi-chassis ready
- Passive optical backplane





COMPASS > **EOS**

COMPASS EOS

THANK YOU

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